

DATA SHEET



SAA5261; SAA5262; SAA5263 10-page intelligent teletext decoders

Product specification
File under Integrated Circuits, IC02

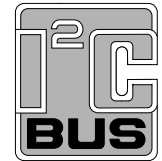
1998 Apr 22

10-page intelligent teletext decoders SAA5261; SAA5262; SAA5263

FEATURES

SAA5261, SAA5262 and SAA5263

- Complete 625-line teletext decoder in a single integrated circuit thereby reducing printed-circuit board area and cost
- Automatic detection of transmitted pages so that only existing pages will be selected by page-up and page-down once inventory validated
- Automatic detection of transmitted Fasttext links or service information (packet 8/30)
- On-screen display for user interface (menus, etc.) using teletext and dedicated menu icons
- Video Programming System (VPS) decoding
- Wide Screen Signalling (WSS) decoding
- 8-page Fasttext decoder
- 6-page TOP decoder in addition to capture of Basic TOP Table (BTT) and 3 Additional Information Table (AIT) pages
- 4-page user defined list mode
- Yugoslavian, Cyrillic, Greek/Turkish, Thai, Arabic/Hebrew, Pan-European and Arabic/English/French language coverage
- High level command interface via I²C-bus giving easy control from a low software overhead
- High level command interface is backward compatible to SAFARI interface
- 625 and 525 line display
- RGB interface to standard colour decoder ICs, push-pull output drive
- Versatile 8-bit open-drain I/O expander
- Single 12 MHz crystal oscillator for reduced cost
- +5 V power supply.



SAA5262 and SAA5263

- Automatic Channel Installation (ACI)
- Enhanced SAFARI interface providing additional commands.

SAA5263

- Electronic Programme Guide (EPG) feature.

GENERAL DESCRIPTION

The SAA526xPS ICs are single-chip 10-page 625-line World System Teletext (WST) decoders with a high level command interface, SAFARI compatible.

It has been designed so that the overall system cost is kept to a minimum. This has been achieved through the capability of the device to be driven from a single +5 V power supply, low cost 12 MHz crystal oscillator and the high level command interface, which offers the benefit of low software overhead in the TV microcontroller.

The SAA526xPS offers automatic detection of Fasttext or TOP transmissions. The device also incorporates a facility to detect the pages in the transmission, which allows only transmitted pages to be selected by page-up and page-down.

SAA5262 and SAA5263 provide Automatic Channel Installation (ACI) information.

SAA5263 provides access to Electronic Programme Guide (EPG) information.

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5261PS	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1
SAA5262PS	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1
SAA5263PS	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	4.5	5.0	5.5	V
$I_{DD(M)}$	microcontroller supply current	–	20	35	mA
I_{DDA}	analog supply current	–	35	50	mA
$I_{DD(T)}$	teletext supply current	–	50	80	mA
f_{xtal}	crystal frequency	–	12	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

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BLOCK DIAGRAM

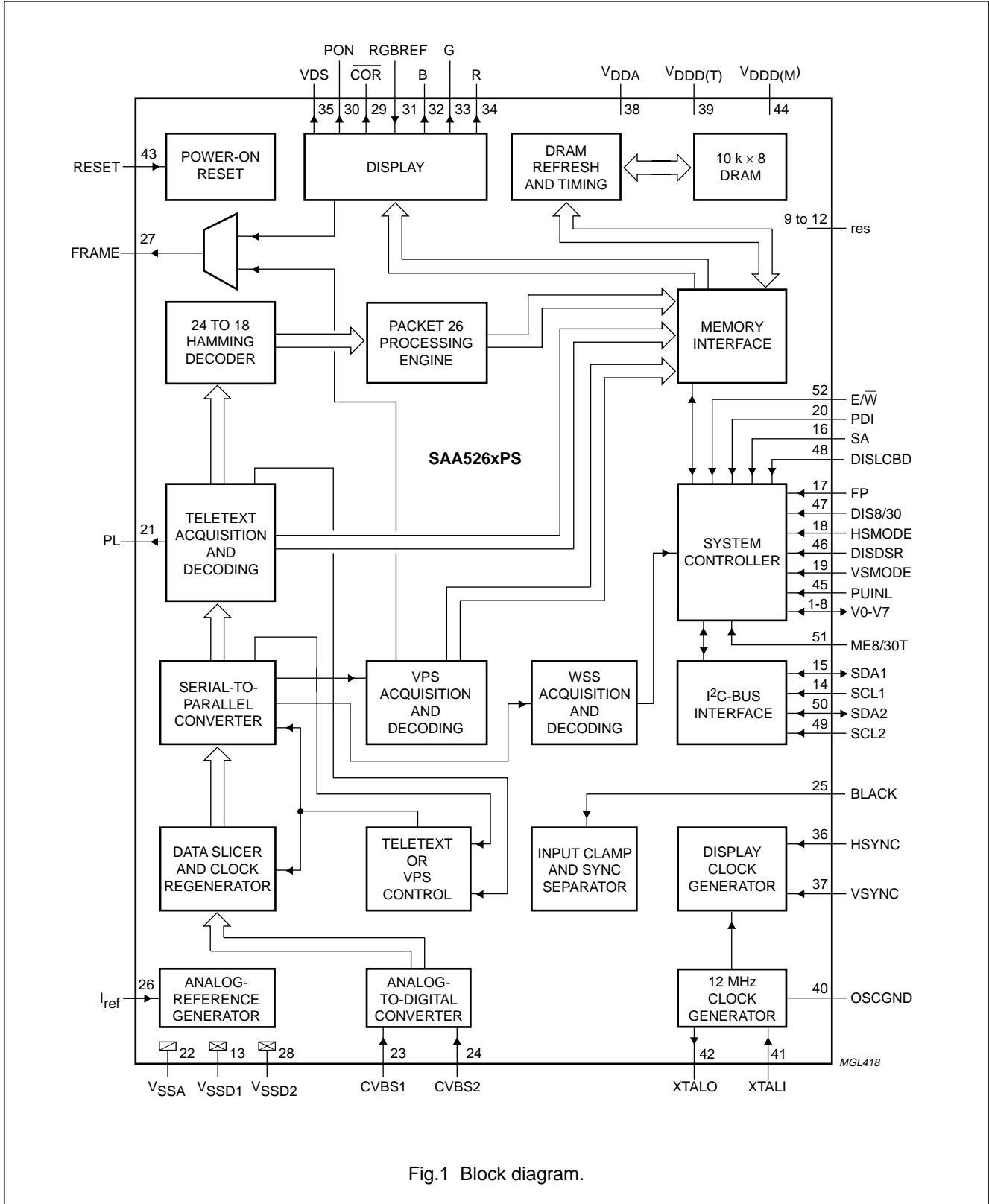


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
V0	1	versatile open-drain input/output bit 0 (should be tied HIGH)
V1	2	versatile open-drain input/output bit 1 (should be tied HIGH)
V2	3	versatile open-drain input/output bit 2 (should be tied HIGH)
V3	4	versatile open-drain input/output bit 3 (should be tied HIGH)
V4	5	versatile open-drain input/output bit 4 (should be tied HIGH)
V5	6	versatile open-drain input/output bit 5 (should be tied HIGH)
V6	7	versatile open-drain input/output bit 6 (should be tied HIGH)
V7	8	versatile open-drain input/output bit 7 (should be tied HIGH)
res	9	reserved
res	10	reserved
res	11	reserved
res	12	reserved
V _{SSD1}	13	digital ground 1
SCLK1	14	serial clock input 1 (NVRAM)
SDAT1	15	serial data input/output 1 (NVRAM)
SA	16	slave address input: LOW selects 58H; HIGH selects 60H
FP	17	field polarity input: LOW selects first half line; HIGH selects second half line at the start of an even field
HSMODE	18	horizontal sync mode control input: LOW selects HSYNC on rising edge
VSMODE	19	vertical sync mode control input. LOW selects VSYNC on rising edge
PDI	20	power-down imminent input: this input should be pulled LOW to indicate that the system is about to lose power
PL	21	phase-lock output: HIGH indicates that the system is phase-locked to the CVBS input
V _{SSA}	22	analog ground
CVBS1	23	CVBS input: this signal is applied via a 100 nF capacitor (nominal input 1 V (p-p))
CVBS2	24	this pin should be connected to ground if unused
BLACK	25	black level input: a 100 nF capacitor should be connected to V _{SSA}
I _{ref}	26	reference current input for analog circuits: for correct operation a 27 kΩ resistor should be connected to V _{SSA}
FRAME	27	Frame output for use in non-interlaced displays: during teletext off, teletext mixed with TV picture and subtitles this pin is inactive. In full teletext mode this pin provides a 25 Hz square wave. FRAME = 1 = odd, FRAME = 0 = even.
V _{SSD2}	28	digital ground 2
COR	29	contrast reduction: active LOW output which allows selective contrast reduction of the television picture to enhance a mixed mode display
PON	30	picture on output: HIGH indicates that a TV picture is present and that the SAA526xPS is in TV mode, mix mode, subtitle mode or news flash mode
RGBREF	31	RGB reference input: drive level reference for RGB outputs
B	32	blue dot rate character output of the blue colour information: the high voltage level is defined by the RGBREF pin (can source 4 mA)

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SYMBOL	PIN	DESCRIPTION
G	33	green dot rate character output of the green colour information: the high voltage level is defined by the RGBREF pin (can source 4 mA)
R	34	red dot rate character output of the red colour information: the high voltage level is defined by the RGBREF pin (can source 4 mA)
VDS	35	push-pull output for blanking the TV picture
HSYNC	36	horizontal sync input: the polarity of this pulse is set by input HSMODE
VSNC	37	vertical sync input: the polarity of this pulse is set by input VSMODE
V _{DDA}	38	analog supply voltage (+5 V)
V _{DDD(T)}	39	digital supply voltage for teletext circuits (+5 V)
OSCGND	40	ground for crystal oscillator
XTALI	41	12 MHz crystal oscillator input
XTALO	42	12 MHz crystal oscillator output
RESET	43	reset input
V _{DDD(M)}	44	digital supply voltage for microcontroller (+5 V)
PUINL	45	power-up in list mode control input: LOW selects auto TOP/Fasttext on power-up; HIGH selects LIST mode on power-up
DISDSR	46	disable default status row input: LOW enables display of status row
DIS8/30	47	disable packet 8/30 display input: LOW enables display of packet 8/30
DISLCBD	48	disable Link Control Byte (LCB) decode input: LOW enables decoding of the LCB in Fasttext
SCLK2	49	serial clock input (I ² C-bus)
SDAT2	50	serial data input/output (I ² C-bus)
ME8/30T	51	mesh 8/30 and time displays input: HIGH will select a meshed display for the packet 8/30 and time
E/ \bar{W}	52	East/West language select input: LOW selects West language

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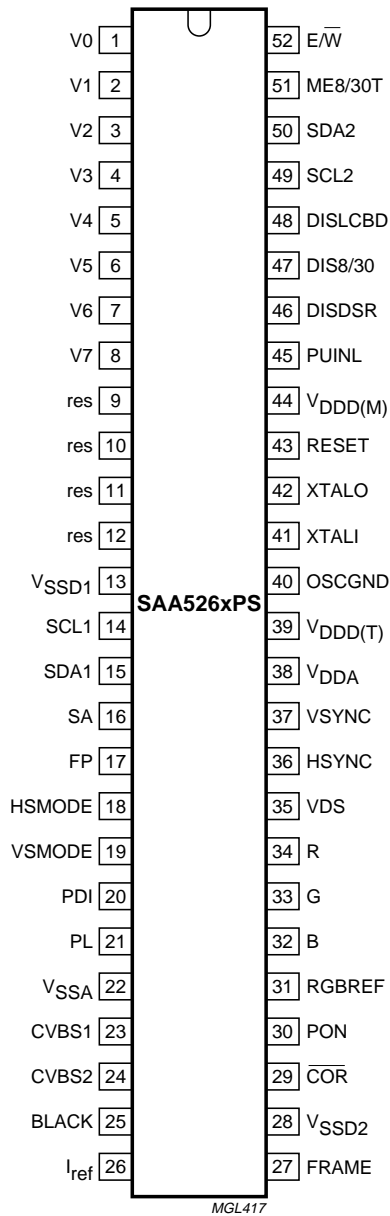


Fig.2 Pin configuration.

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HIGH LEVEL COMMAND INTERFACE

The I²C-bus interface is used to pass control commands and data between the SAA526xPS and the television microcontroller. The interface uses high level commands, which are backward compatible with the SAFARI interface.

The formats for the I²C-bus transmission are as follows:

Table 1 User command

START	I ² C-bus ADDRESS	WRITE	ACK	COMMAND	ACK	STOP
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Table 2 System command

START	I ² C-bus ADDRESS	WRITE	ACK	COMMAND	ACK	PARAMETER	ACK	STOP
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Table 3 System read

START	I ² C-bus ADDRESS	READ	ACK	DATA	NACK	STOP
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Table 4 I²C-bus address

PIN 16 = LOW		PIN 16 = HIGH	
ADDRESS	DESCRIPTION	ADDRESS	DESCRIPTION
01 01 100	read = 1; write = 0	0110 000	read = 1; write = 0

Table 5 Control commands

COMMAND BYTE (HEX)	DATA BYTE	COMMAND DESCRIPTION	COMMAND BYTE (HEX)	DATA BYTE	COMMAND DESCRIPTION
03	–	picture	1F	–	program 15
04	–	TV status	20	–	red
07	–	time	21	–	green
10	–	program 0	22	–	yellow
11	–	program 1	23	–	subtitle
12	–	program 2	24	–	text status
13	–	program 3	25	–	hold
14	–	program 4	26	–	reveal
15	–	program 5	27	–	cancel
16	–	program 6	28	–	index
17	–	program 7	29	–	list toggle
18	–	program 8	2B	–	reveal toggle
19	–	program 9	2C	–	store
1A	–	program 10	2D	–	previous
1B	–	program 11	2F	–	subcode
1C	–	program 12	30	–	digit 1
1D	–	program 13	31	–	digit 2
1E	–	program 14	32	–	digit 3

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COMMAND BYTE (HEX)	DATA BYTE		COMMAND DESCRIPTION
33	–		digit 4
34	–		digit 5
35	–		digit 6
36	–		digit 7
37	–		digit 8
38	–		digit 9
39	–		digit 0
3A	–		size
3B	–		up
3C	–		down
3D	–		cyan
3E	–		mix
3F	–		text
4A	0		read PAL + line
89	00 to 41		select list
91	00 to 03 or 00 to 80		force mode
92	00		read broadcast status
93	00 or 01		read network identification
94	0		read PCS byte
98	OSD data		OSD mode on
99	0		OSD mode off
9A	0		OSD display on
9B	0		OSD display off
9C	0		OSD cursor on
9D	0		OSD cursor off
9E	0, row, column		OSD position
9F	0 followed by 20 bytes		OSD data write
A0	00 to FF		bitwise parameter or V7 to V0
A1	00 to FF		bitwise parameter and V7 to V0
A2	00 to FF		returns V7 to V0 on I ² C-bus read
A3	PWM No.	PWM data	PWM control
B0	reg	data	or text register
B1	reg	data	and text register
B2	reg	data	read text register
B8	0		quick list

COMMAND BYTE (HEX)	DATA BYTE	COMMAND DESCRIPTION
SAA5262 and SAA5263 only		
B9	0	get time
C0	0 = disable	set ACI mode
	1 = enable	
C1	0	get ACI status
C2	0	select next ACI channel
C3	information type	get ACI information
D0	0	get device version
D1	page type and page number	set page number
D2	page type	get page number
D3	page type and language	set language
D4	page type	get language
D5	row 24 control	enable/disable row 24
D6	start column and length string	set row 24 contents
D7	string type, index length and string	set string contents
D8	option type and values	set option
D9	movement type	move cursor
SAA5263 only		
C8	EPG mode	set EPG mode
C9	0	get EPG status
CA	number and list of features	set EPG feature list
CB	0	get number of EPG CNIs found
CC	CNI index	get found EPG CNIs
CD	number and list of CNIs	set EPG CNI list
CE	table type, item type and string index	get EPG item information

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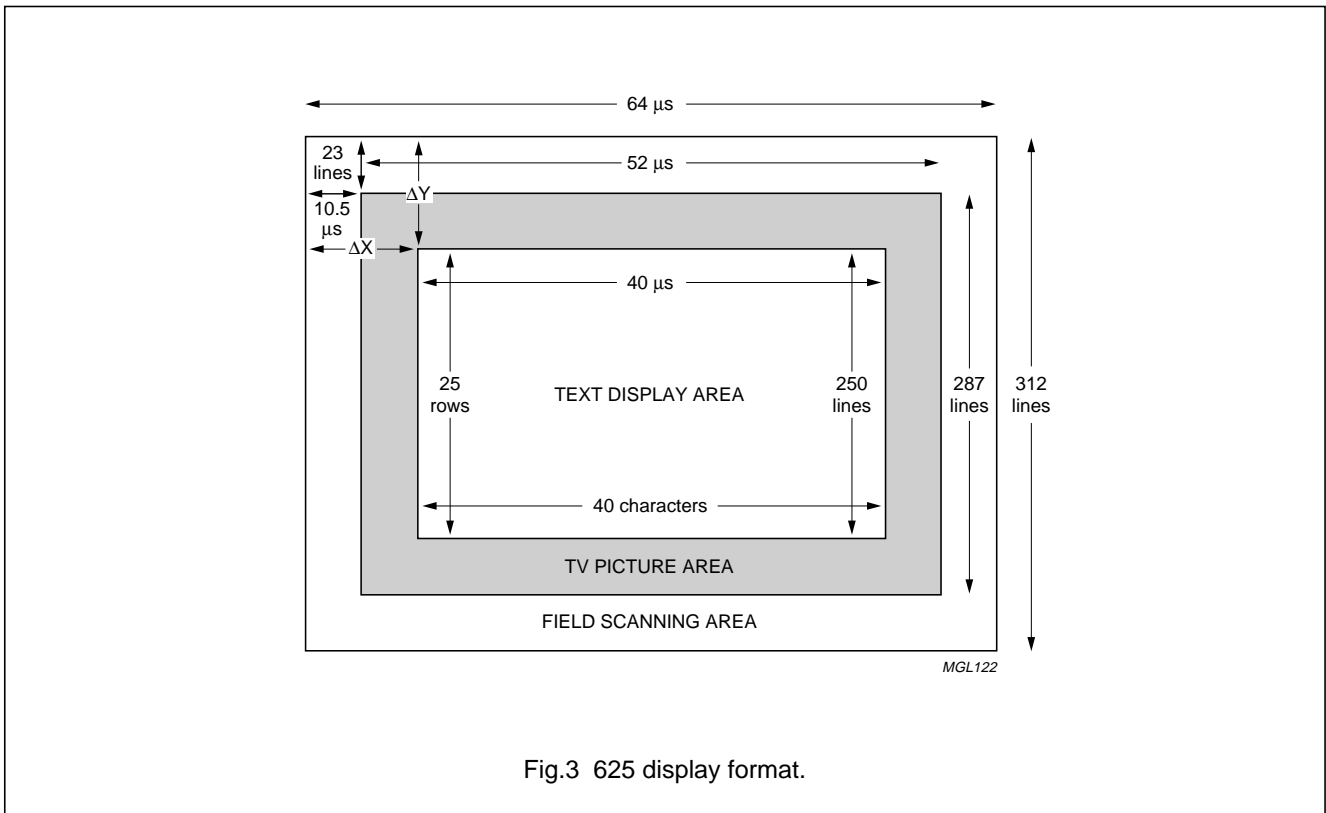


Fig.3 625 display format.

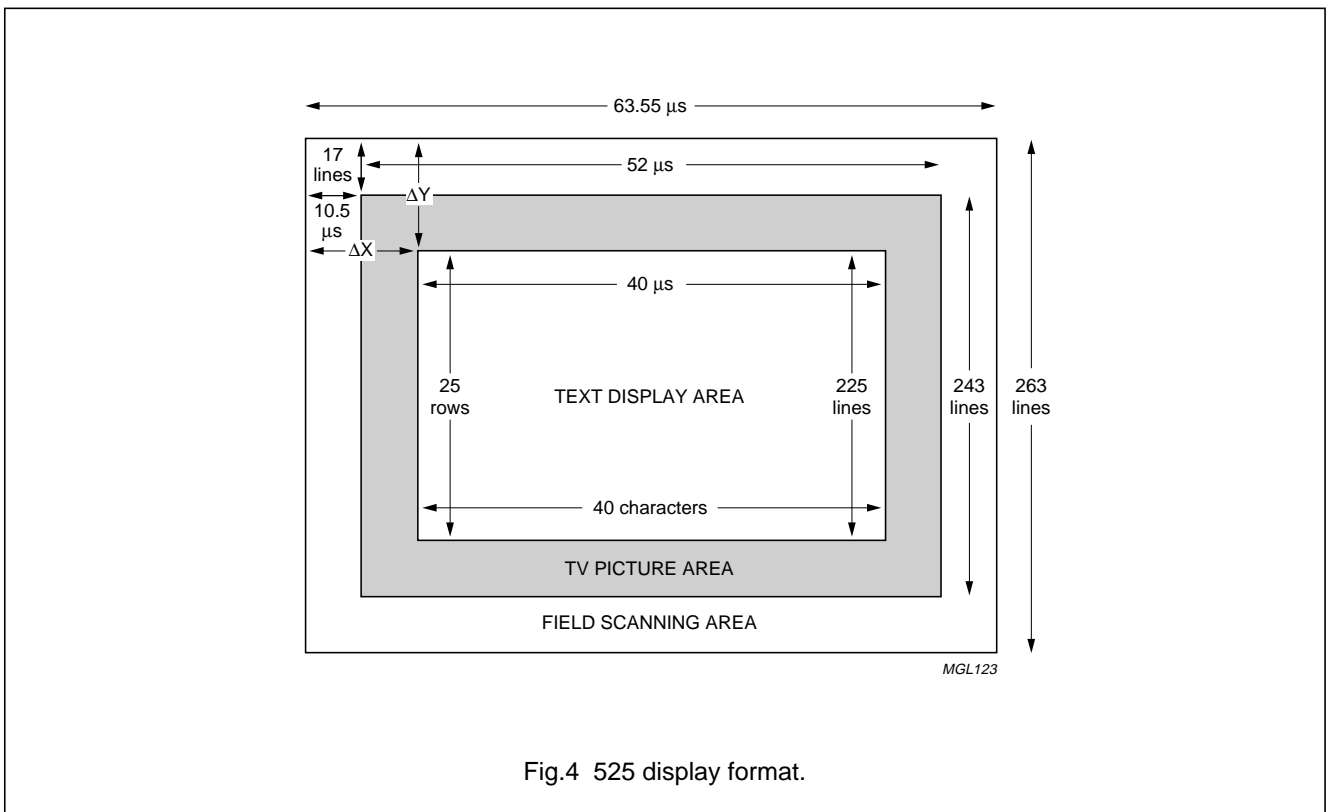


Fig.4 525 display format.

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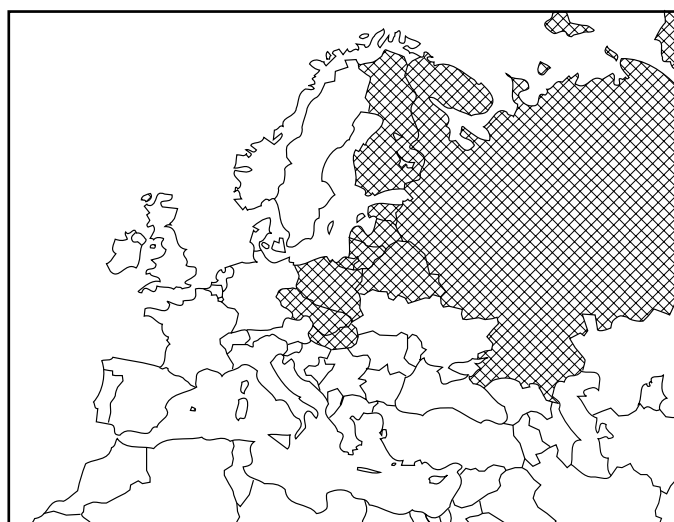
CHARACTER SETS

Geographical coverage



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Fig.5 SAA5261PS/101 Yugoslavia.

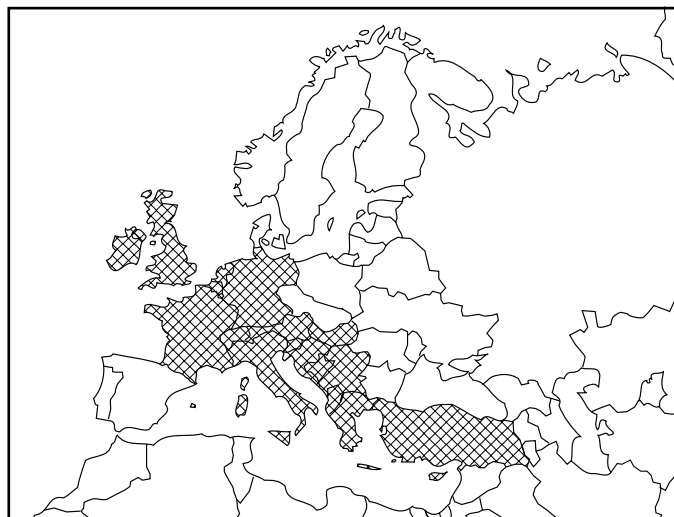


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Fig.6 SAA5261PS/109 Cyrillic, SAA5262PS/122 Cyrillic.

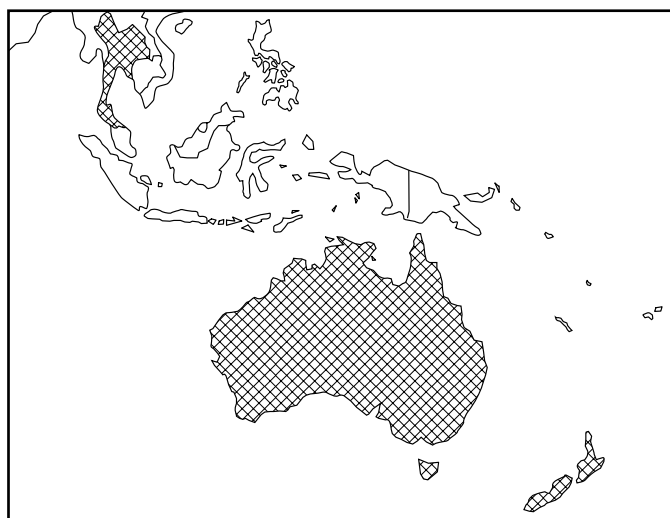
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MGL129

Fig.7 SAA5261/113 Greek/Turkish, SAA5262PS/123 Greek/Turkish.

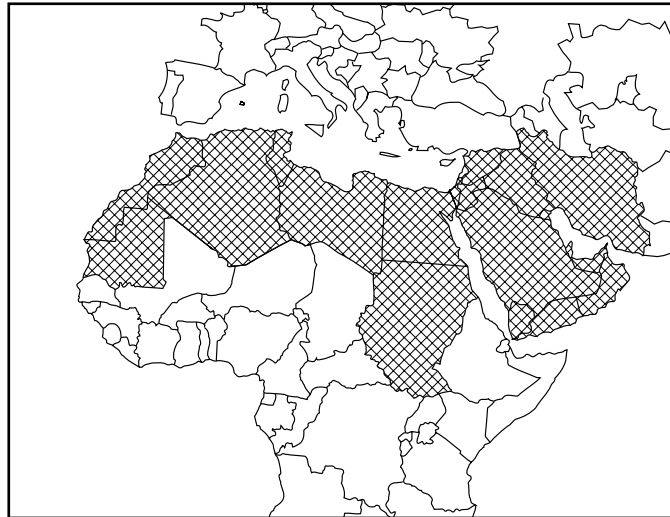


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Fig.8 SAA5261PS/104 Thai, SAA5262PS/124 Thai.

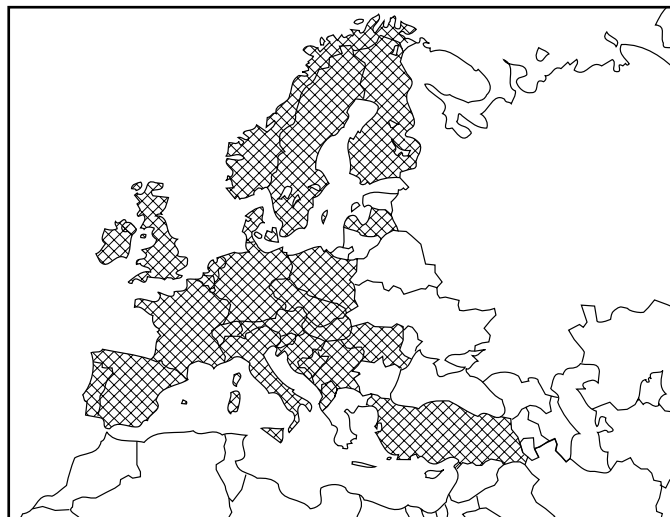
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Fig.9 SAA5261P/105 Arabic/Hebrew, SAA5262PS/125 Arabic/Hebrew.

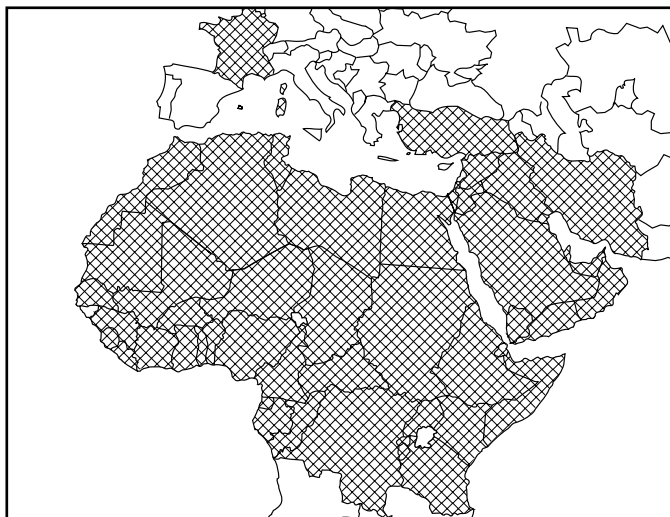


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Fig.10 SAA5261PS/117 Pan-European, SAA5262PS/128 Pan-European/Eastern, SAA5263PS/137 Pan-European.

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Fig.11 SAA5261PS/108 Arabic/English/French, SAA5262PS/126 Arabic/English/French.



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Fig.12 SAA5261PS/110 Iranian, SAA5262PS/120 Iranian.

The character sets for the languages Yugoslavian, Cyrillic, Greek/Turkish, Thai, Arabic/Hebrew, Pan-European, Arabic/English/French and Iranian are available on request.

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LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DDD}	digital supply voltages		-0.3	+6.5	V
V _{DDA}	analog supply voltage		-0.3	+6.5	V
V _I	input voltage (any input)	note 1	-0.3	V _{DDD(M)} + 0.5	V
V _O	output voltage (any output)	note 1	-0.3	V _{DDD(M)} + 0.5	V
I _O	output current (each output)		-	±10	mA
I _{I/OK}	DC input or output diode current		-	±20	mA
T _{amb}	operating ambient temperature		-20	+70	°C
T _{stg}	storage temperature		-55	+125	°C

Note

1. This maximum value has an absolute maximum of 6.5 V independent of V_{DDD}.

QUALITY AND RELIABILITY

This device will meet Philips Semiconductors general quality specification for business group "Consumer Integrated Circuits SNW-FQ-611-Part E". The principal requirements are shown in Tables 6 to 9.

Group A**Table 6** Acceptance tests per lot; note 1

TEST	REQUIREMENTS
Mechanical	cumulative target: <80 ppm
Electrical	cumulative target: <80 ppm

Note

1. ppm = fraction of defective devices, in parts per million.

Group B**Table 7** Processability tests (by package family); note 1

TEST	REQUIREMENTS
Solderability	<7% LTPD
Mechanical	<15% LTPD
Solder heat resistance	<15% LTPD

Note

1. LTPD = Lot Tolerance Percent Defective.

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Group C**Table 8** Reliability tests (by package family); note 1

TEST	CONDITIONS	REQUIREMENTS
Operational life	168 hours at $T_j = 150\text{ °C}$	<1000 FPM at $T_j = 70\text{ °C}$
Humidity life	temperature, humidity, bias 1000 hours, $T_{amb} = 85\text{ °C}$, 85% RH (or equivalent test)	<2000 FPM
Temperature cycling performance	$T_{stg(min)}$ to $T_{stg(max)}$	<2000 FPM

Note

1. FPM = fraction of devices failing at test conditions, in Failures Per Million.

Table 9 Reliability tests (by device type)

TEST	CONDITIONS	REQUIREMENTS
ESD and latch-up	ESD human body model 100 pF, 1.5 k Ω	<2000 V
	ESD machine model 200 pF, 0 Ω	<200 V
	latch-up	100 mA, 1.5V _{DD} (absolute maximum)

CHARACTERISTICS

$V_{DD(M)} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$; $T_{amb} = -20\text{ to }+70\text{ °C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DD(M)}$	microcontroller supply voltage	referenced to V_{SS}	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage	referenced to V_{SS}	4.5	5.0	5.5	V
$V_{DD(T)}$	teletext supply voltage	referenced to V_{SS}	4.5	5.0	5.5	V
$I_{DD(M)}$	microcontroller supply current		–	20	35	mA
I_{DDA}	analog supply current		–	35	50	mA
$I_{DD(T)}$	teletext supply current		–	50	80	mA
Digital inputs						
PIN RESET						
V_{IL}	LOW-level input voltage		–0.3	–	$0.2V_{DD(M)} - 0.1$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD(M)}$	–	$V_{DD(M)} + 0.3$	V
I_{LI}	input leakage current	$V_i = 0\text{ to }V_{DD(M)}$	–10	–	+10	μA
C_i	input capacitance		–	–	4	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PINS HSYNC AND VSYNC						
$V_{th(f)}$	switching threshold falling		$0.2V_{DD(M)}$	–	–	V
$V_{th(r)}$	switching threshold rising		–	–	$0.8V_{DD(M)}$	V
V_{hys}	hysteresis voltage		–	$0.33V_{DD(M)}$	–	V
C_i	input capacitance		–	–	4	pF
Digital outputs						
PINS R, G AND B: note 1						
V_{OL}	LOW-level output voltage	$I_{OL} = 2 \text{ mA}$	0	–	0.2	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -2 \text{ mA}$	$V_{RGBREF} - 0.3$	V_{RGBREF}	$V_{RGBREF} + 0.4$	V
$ Z_O $	output impedance		–	–	150	Ω
C_L	load capacitance		–	–	50	pF
I_O	DC output current		–	–	–4	mA
$t_{o(r)}$	output rise time	between 10 and 90%; $C_L = 50 \text{ pF}$	–	–	20	ns
$t_{o(f)}$	output fall time	between 90 and 10%; $C_L = 50 \text{ pF}$	–	–	20	ns
PIN VDS						
V_{OL}	LOW-level output voltage	$I_{OL} = 1.6 \text{ mA}$	0	–	0.2	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -1.6 \text{ mA}$	$V_{DD(M)} - 0.3$	–	$V_{DD(M)} + 0.4$	V
C_L	load capacitance		–	–	50	pF
$t_{o(r)}$	output rise time	between 10 and 90%; $C_L = 50 \text{ pF}$	–	–	20	ns
$t_{o(f)}$	output fall time	between 90 and 10%; $C_L = 50 \text{ pF}$	–	–	20	ns
PINS R, G, B AND VDS						
$t_{d(skew)}$	skew delay between any two pins		–	–	20	ns
PIN \overline{COR} (OPEN-DRAIN OUTPUT)						
V_{OH}	HIGH-level pull-up output voltage		–	–	$V_{DD(M)}$	V
V_{OL}	LOW-level output voltage	$I_{OL} = 2 \text{ mA}$	0	–	0.5	V
I_{OL}	LOW-level output current		–	–	2	mA
C_L	load capacitance		–	–	25	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PIN FRAME						
V _{OH}	HIGH-level output voltage	I _{OL} = 8 mA	0	–	0.5	V
V _{OL}	LOW-level output voltage	I _{OL} = –8 mA	V _{DD(M)} – 0.5	–	V _{DD(M)}	V
I _{OL}	LOW-level output current		–8	–	+8	mA
C _L	load capacitance		–	–	100	pF
Digital inputs/outputs						
PINS V0 TO V7						
V _{IL}	LOW-level input voltage		–0.3	–	0.2V _{DD(M)} – 0.1	V
V _{IH}	HIGH-level input voltage		3.0	–	V _{DD(M)} + 0.3	V
C _i	input capacitance		–	–	4	pF
V _{OL}	LOW-level output voltage	I _{OL} = 10 mA	0	–	0.45	V
C _L	load capacitance		–	–	50	pF
PINS SCL AND SDA (PINS 14, 15, 49 AND 50)						
V _{IL}	LOW-level input voltage		–0.3	–	+1.5	V
V _{IH}	HIGH-level input voltage		3.0	–	V _{DD(M)} + 0.3	V
C _i	input capacitance		–	–	5	pF
V _{OL}	LOW-level output voltage	I _{OL} = 3 mA	0	–	0.5	V
C _L	load capacitance		–	–	400	pF
t _{o(f)}	output fall time	between 3 and 1 V	–	–	200	ns
Digital inputs						
PINS VSMODE, HSMODE, PDI, SA, FP, PUINL, DISDSR, DIS8/30, DISLCBD, ME8/30T AND E\bar{W}						
V _{IL}	LOW-level input voltage		–0.3	–	0.2V _{DD(M)} – 0.1	V
V _{IH}	HIGH-level input voltage		0.2V _{DD(M)} + 0.9	–	V _{DD(M)} + 0.3	V
C _i	input capacitance		–	–	4	pF
C _L	load capacitance		–	–	50	pF
Digital outputs						
PINS PL AND PON						
V _{OL}	LOW-level output voltage	I _{OL} = 10 mA	0	–	0.45	V
C _L	load capacitance		–	–	50	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs						
PINS CVBS0 AND CVBS1						
V_{sync}	sync voltage amplitude		0.1	0.3	0.6	V
$V_{\text{vid(p-p)}}$	video input voltage amplitude (peak-to-peak value)		0.7	1.0	1.4	V
Z_{source}	source impedance		–	–	250	Ω
V_{IH}	HIGH-level input voltage		3.0	–	$V_{\text{DDD(M)}} + 0.3$	V
$ Z_{\text{i}} $	input impedance		2.5	5.0	–	k Ω
C_{i}	input capacitance		–	–	10	pF
PIN I_{ref}						
R_{VSS}	resistor to ground		–	27	–	k Ω
RGBREF: note 1						
V_{i}	input voltage		–0.3	–	$V_{\text{DDD(M)}}$	V
I_{i}	DC input current		–	–	12	mA
Analog input/output						
PIN BLACK						
C_{BLACK}	storage capacitor to ground		–	100	–	nF
V_{BLACK}	black level voltage for nominal sync amplitude		1.8	2.15	2.5	V
I_{LI}	input leakage current		–10	–	+10	μA
Crystal oscillator						
PIN XTALI						
V_{IL}	LOW-level input voltage		–0.3	–	$0.2V_{\text{DDD(M)}} - 0.1$	V
V_{IH}	HIGH-level input voltage		$0.7V_{\text{DDD(M)}}$	–	$V_{\text{DDD(M)}} + 0.3$	V
C_{i}	input capacitance		–	–	10	pF
PIN XTALO						
C_{o}	output capacitance		–	–	10	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CRYSTAL SPECIFICATION: note 2						
f _{xtal}	nominal frequency		–	12	–	MHz
C _L	load capacitance		–	32	–	pF
C1	series capacitance	T _{amb} = 25 °C	–	18.5	–	fF
C0	parallel capacitance	T _{amb} = 25 °C	–	4.9	–	pF
R _{res}	resonance resistance	T _{amb} = 25 °C	–	35	–	Ω
T _{xtal}	temperature range		–20	+25	+70	°C
X _j	adjustment tolerance	T _{amb} = 25 °C	–	–	±50 × 10 ^{–6}	
X _d	drift		–	–	±30 × 10 ^{–6}	

Notes

1. All RGB current is sourced from the RGBREF pin. The maximum effective series resistance between RGBREF and the R, G and B pins is 150 Ω.
2. Crystal order number 4322 143 05561.

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	INPUT	OUTPUT	I ² C-BUS SPECIFICATION
SCL timing				
t _{HD;STA}	START condition hold time	≥4.0 μs	note 1	≥4.0 μs
t _{LOW}	SCL LOW time	≥4.7 μs	note 1	≥4.7 μs
t _{HIGH}	SCL HIGH time	≥4.0 μs	≥4.0 μs; note 2	≥4.0 μs
t _{r(SCL)}	SCL rise time	≤1.0 μs	note 3	≤1.0 μs
t _{f(SCL)}	SCL fall time	≤0.3 μs	≤0.3 μs; note 4	≤0.3 μs
SDA timing				
t _{SU;DAT1}	data set-up time	≥250 ns	note 1	≥250 ns
t _{HD;DAT}	data hold time	≥0 ns	note 1	≥0 ns
t _{SU;STA}	repeated START set-up time	≥4.7 μs	note 1	≥4.7 μs
t _{SU;STO}	STOP condition set-up time	≥4.0 μs	note 1	≥4.0 μs
t _{BUF}	bus free time	≥4.7 μs	note 1	≥4.7 μs
t _{r(SDA)}	SDA rise time	≤1.0 μs	note 3	≤1.0 μs
t _{f(SDA)}	SDA fall time	≤0.3 μs	≤0.3 μs; note 4	≤0.3 μs

Notes

1. This parameter is determined by the user software. It must comply with the I²C-bus specification.
2. This value gives the auto-clock pulse length which meets the I²C-bus specification for the special crystal frequency. Alternative, the SCL pulse must be timed by software.
3. The rise time is determined by the external bus line capacitance and pull-up resistor. It must be less than 1 μs.
4. The maximum capacitance on bus lines SDA and SCL is 400 pF.

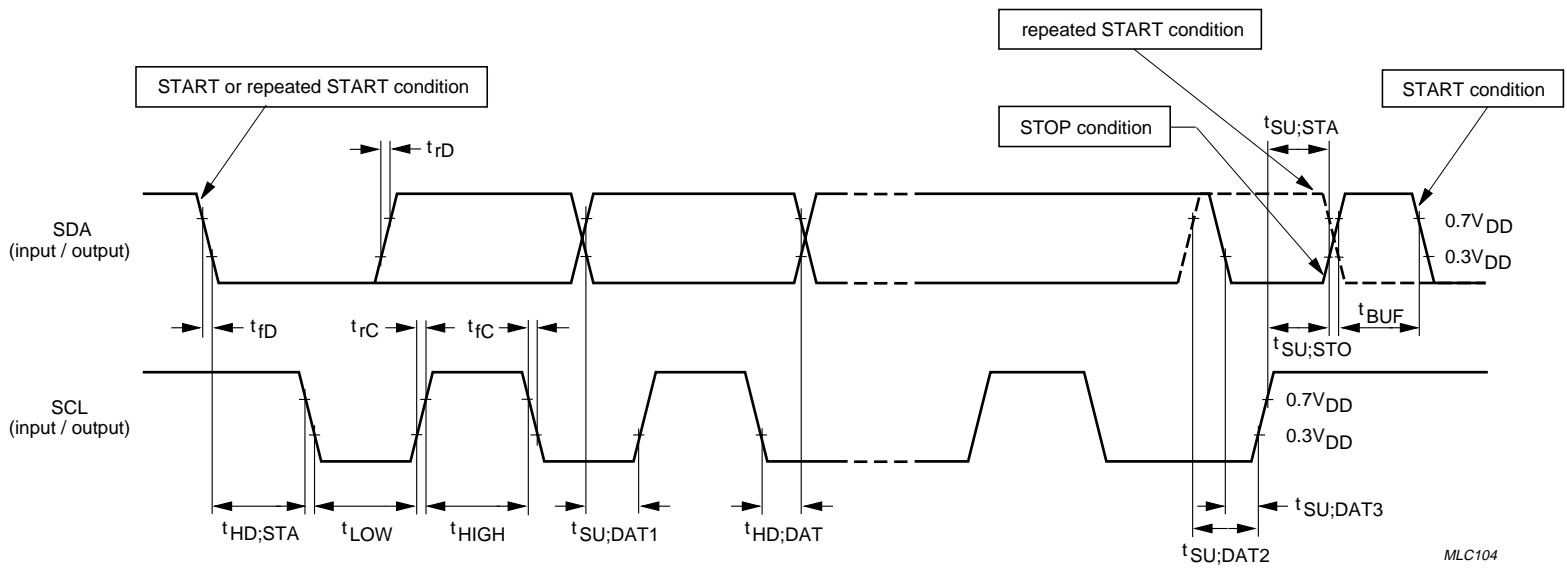


Fig.13 I²C-bus interface timing.

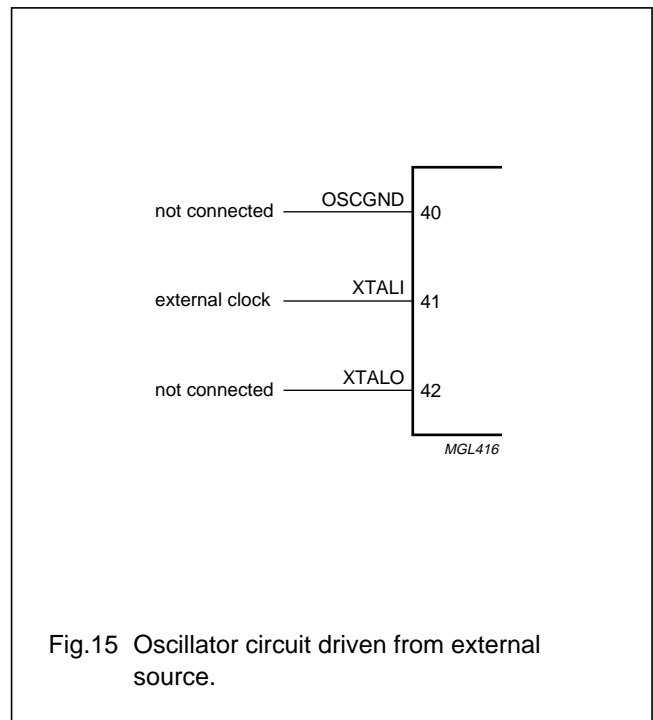
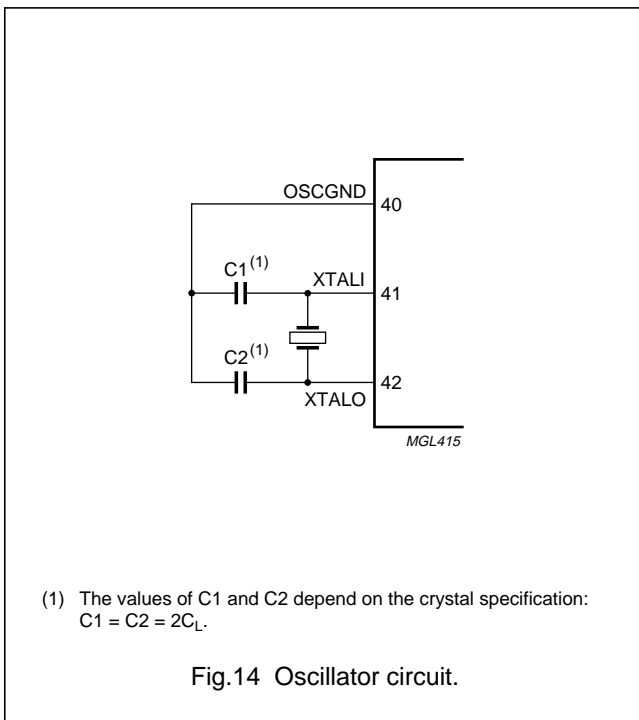
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CLOCK GENERATOR

The oscillator circuit is a single-stage inverting amplifier in a Pierce oscillator configuration. The circuitry between pins XTALI and XTALO is basically an inverter biased to the transfer point. A crystal must be used as the feedback element to complete the oscillator circuitry. It is operated in parallel resonance. XTALI is the high gain amplifier input and XTALO is the output.

To drive the device externally XTALI is driven from an external source and XTALO is left open-circuit.



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EMC GUIDELINES

Optimization of circuit return paths and minimisation of common mode noise will be assisted by using a double-sided PCB with a low inductance ground plane.

On a single-sided PCB a local ground plane under the whole IC should be present, as shown in Fig.16. This should be connected by the widest possible connection back to the PCB ground connection and bulk electrolytic decoupling capacitor. It should preferably not connect to other grounds on the way and no wire links should be present in this connection. The use of wire links increases ground bounce by introducing inductance into the ground.

The supply pins can be decoupled at the pin to the ground plane under the IC. This is easily accomplished using surface mount capacitors, which are more effective than leaded components at high frequency. Using a device socket will unfortunately add to the area and inductance of the external bypass loop.

A ferrite bead or inductor with resistive characteristics at high frequency may be utilized in the supply line close to the decoupling capacitor to provide a high impedance. To prevent pollution by conduction onto signal lines (which may then radiate) signals connected to the +5 V supply via a pull up resistor should not be connected to the IC side of the ferrite component.

OSCGND should be connected only to the crystal load capacitors and not the local or circuit ground.

Keep physical connection distances to associated active devices short.

Route output traces with close proximity mutually coupled ground return paths.

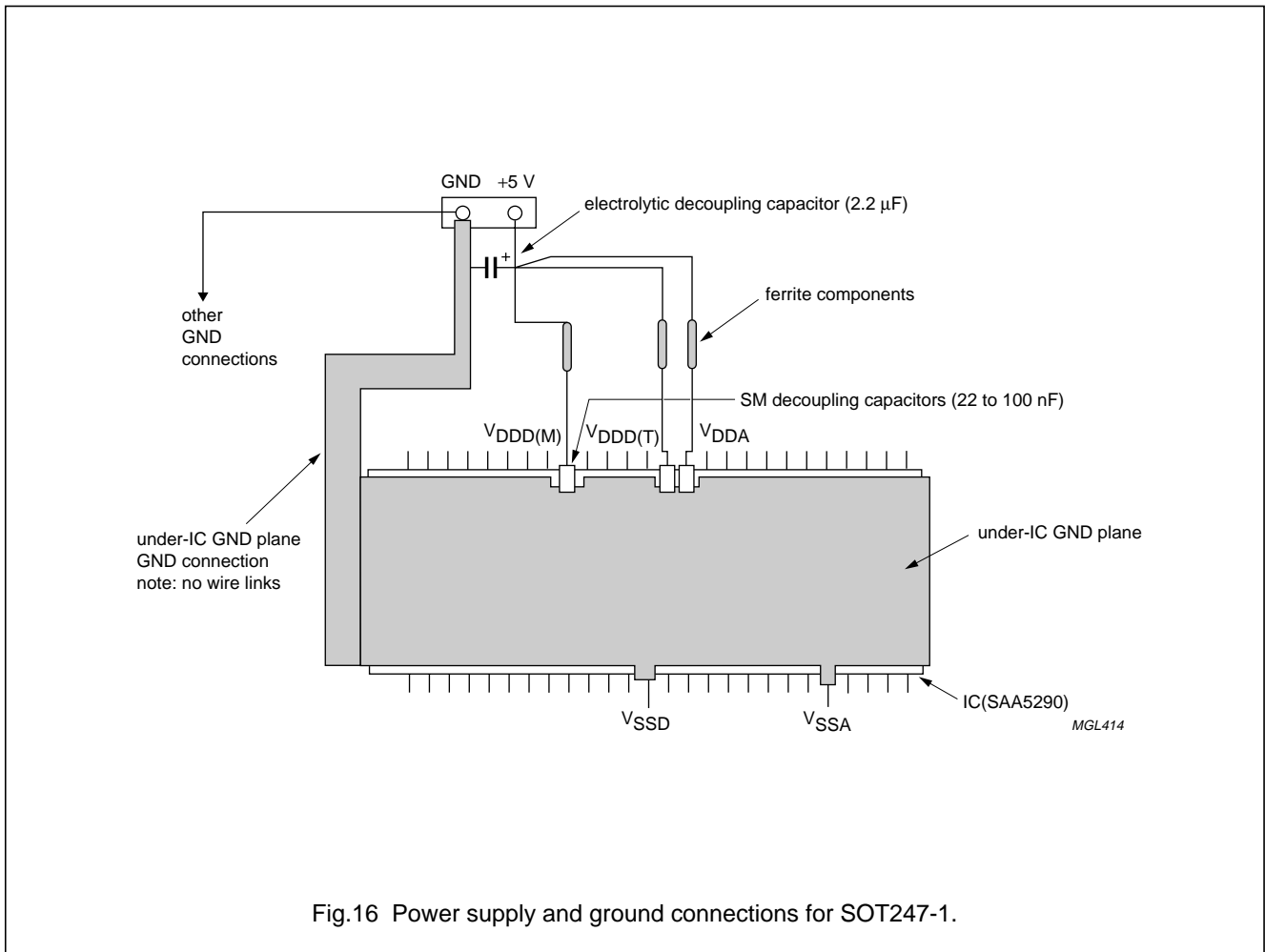


Fig.16 Power supply and ground connections for SOT247-1.

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APPLICATION INFORMATION

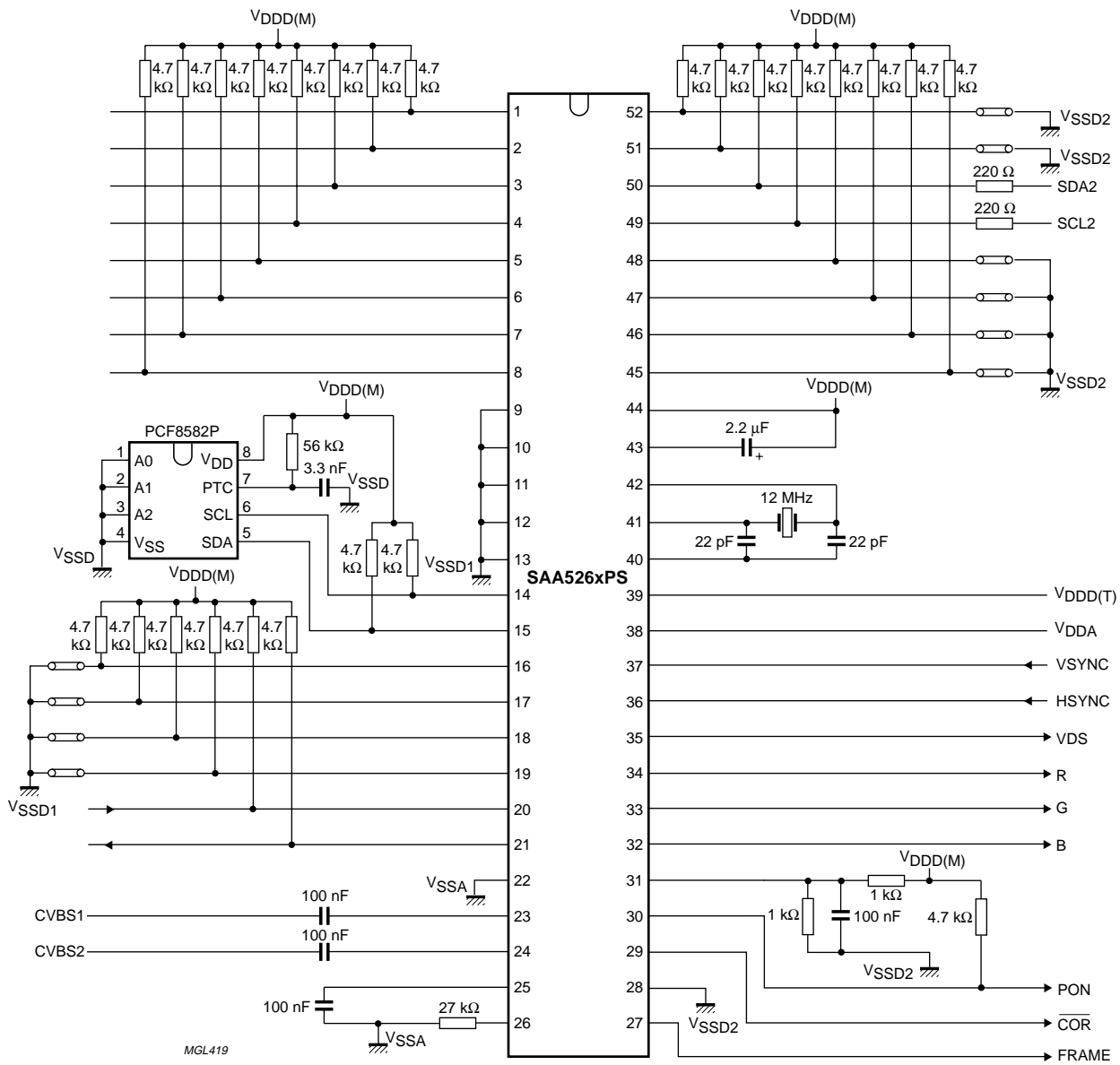


Fig.17 Application diagram.

MGL419

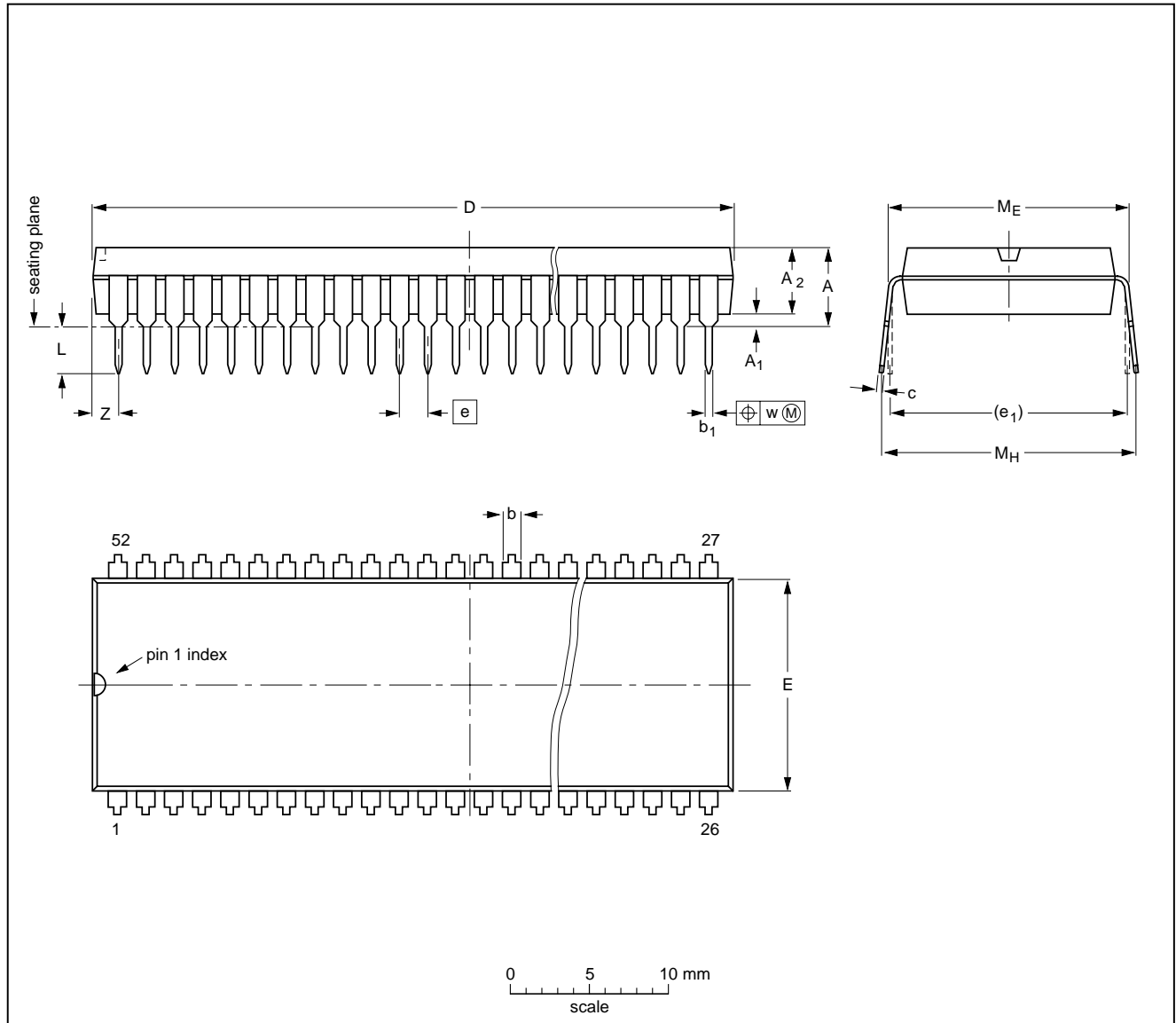
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PACKAGE OUTLINE

SDIP52: plastic shrink dual in-line package; 52 leads (600 mil)

SOT247-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	z ⁽¹⁾ max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	47.9 47.1	14.0 13.7	1.778	15.24	3.2 2.8	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT247-1						90-01-22 95-03-11

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SOLDERING**Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact

with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
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Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

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Tel. +359 2 689 211, Fax. +359 2 689 102

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China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
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Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
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Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

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Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
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South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
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Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

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Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
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For all other countries apply to: Philips Semiconductors,
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